



NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

Revision 1.1: Update DEVICE ORDER INFORMATION

Revision 1.2: Update ABS T_J max and internal soft-start time in FEATURES, add MSL information, and remove information related to SCT2231TVAR

KN AN= HA ARE A	L= G=CEJC PULA	OP= J =N L= GMPU	L= G=CA I =NGEJC	LEJO	L= G=CA AO NÆPÆJ	I OH
SCT2231TVB32nt						

J=I A	LEJ	LEJ BQJ PÆJ
GND	1	Power ground. Must be soldered directly to ground plane.
SW	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	5	Enable logic input. Floating the pin enables the device. The device has precision enable thresholds 1.2V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

Over operating free-air temperature range unless otherwise noted

L= N= I APAN	ABEJ PÆJ	I EJ	I =T	QJÆ
V _{IN}	Input voltage range	4.2	17	V
T _J	Operating junction temperature	-40	125	°C

L= N= I APAN	ABEJ PÆJ	I EJ	I =T	QJÆ
V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins ⁽¹⁾	-0.5	+0.5	kV

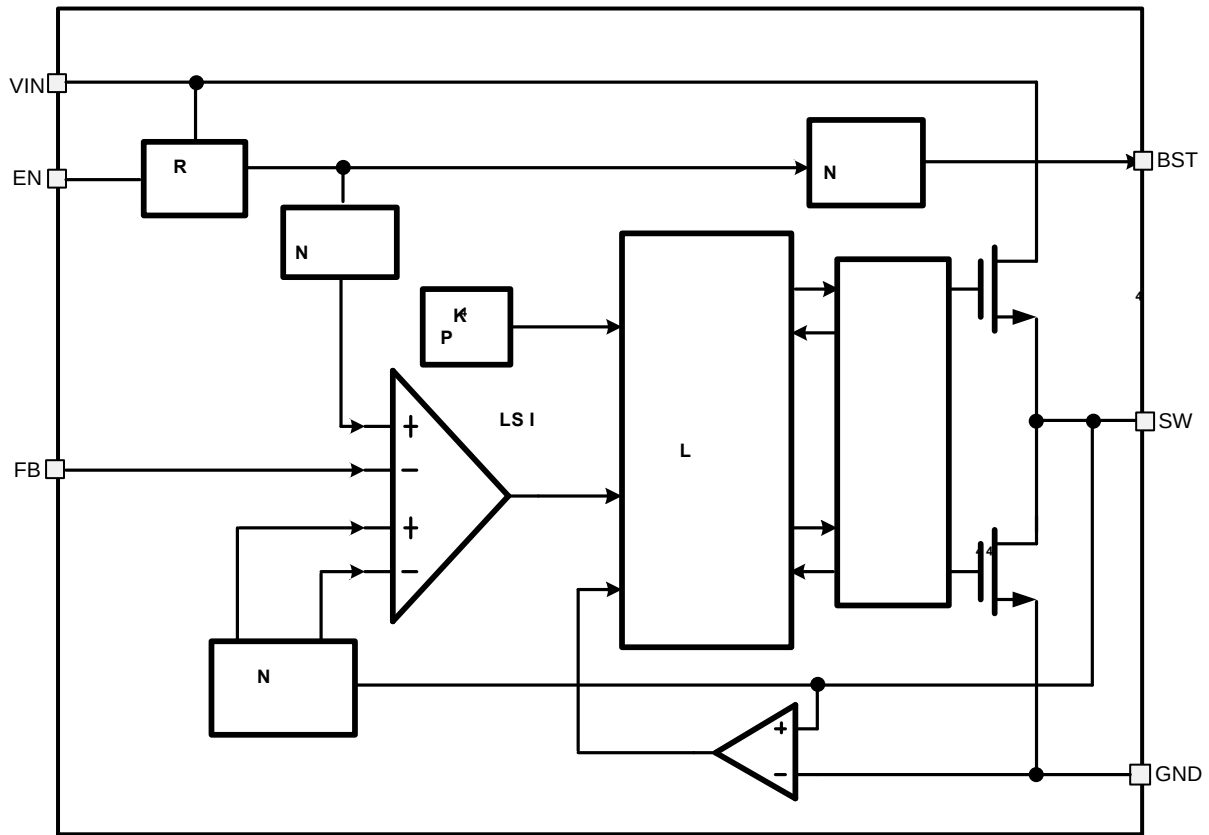
O P. / -

$V_{IN}=12V$, $T_J=-40^{\circ}C\sim 125^{\circ}C$, typical values are tested under $25^{\circ}C$.

QUI	KH	L= N= I APAN	PAOP KJ PEKJ	I E	PUL	I =T	QJP
K							
V_{IN}	Operating input voltage			4.2		17	V
V_{IN_UVLO}	Hysteresis		V_{IN} rising		4.0	4.15	V

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B . R R REJ



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The SCT2231 device is 4.2-17V input, 3A output, and synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time

by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2231 turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2231 turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Where:

VOUT is the output voltage.

VIN is the input voltage.

fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 200ns typical.

B L S I BLS I

The SCT2231 is designed with Forced Pulse Width Modulation (FPWM) at light load conditions for small output voltage ripple. In light load, the inductor current falls below 0A, the buck converter operates at forced continuous current mode. The SCT2331 operates at quasi 750kHz switching frequency.

REJ L

The SCT2231 is designed to operate from an input voltage supply range between 4.2V to 17V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

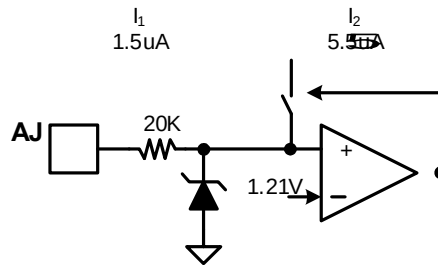
Q R H QRHK

The SCT2231 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.9V with VIN rising and shutdown threshold is 3.6V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

A O

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2231 enables all functions and the device starts soft-start phase. The SCT2231 has the built in 2ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 5.3uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (2) and (3).



B 3 = REJ QRHK

$$3 = \frac{(---) -}{1 (1 - ---) + 2} \quad (2)$$

$$4 = \frac{3 \times}{- + 3 (1 + 2)} \quad (3)$$

Where:

Vstart: Vin rise threshold to enable the device
 Vstop: Vin fall threshold to disable the device
 $I_1=1.5\mu A$
 $I_2=5.3\mu A$
 $V_{ENR}=1.18V$
 $V_{EMF}=1.1V$

K L K L D I

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will dropped below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles soft-start period.

R N

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET yh.C4ers dri-9(v)er.

ripple less than 100mV. Generally, a 25V/10uF input

O P. . / -

K B N O

The SCT2231 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (7) to calculate the resistor divider values.

$$V_1 = \frac{(V_{DD} - V_{FB}) \times R_2}{R_1 + R_2} \quad (7)$$

$$R_1 = \frac{V_{DD} - V_{FB}}{V_{FB} - V_{FB}} \times R_2$$

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REJ9-. R(KQP9/=

B -, OS S K N
REJ9-. R(KQP9-, =

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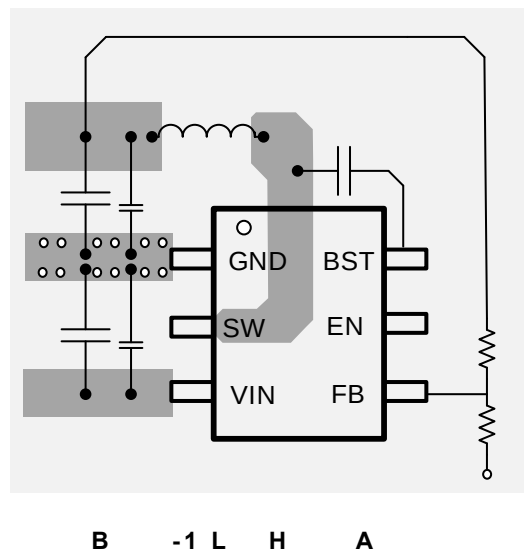
B -- L Q
REJ9- [KQP9 []]

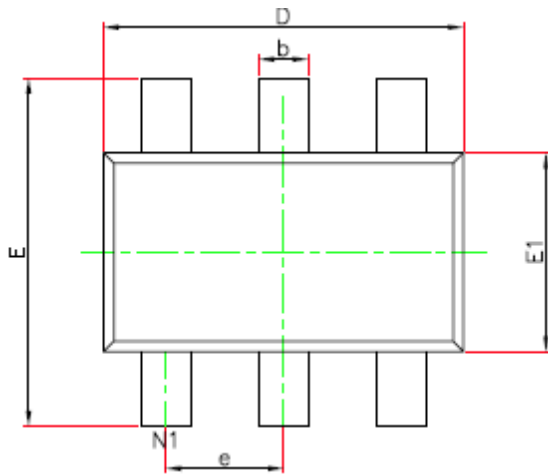


H C

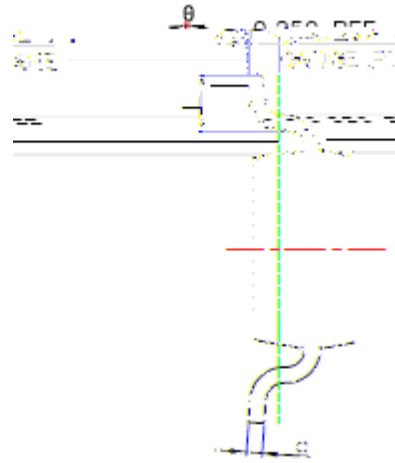
The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15 is the recommended PCB layout of SCT2231.

The layout needs to be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

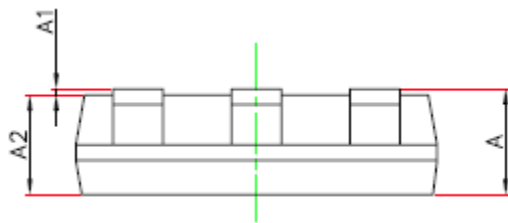




TSOT23-6 TOP VIEW



TSOT23-6 BOTTOM VIEW



TSOT23-6 SIDE VIEW

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A		-----		1.10

JKPA6

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

