NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev 1.0: Release to market

Rev 1.1: Update pin functions and 5V output voltage recommended feedback resistor

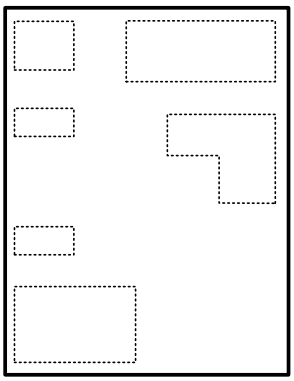
Rev 1.2: Update DEVICE ORDER INFORMATION

Rev 1.3: Update DEVICE ORDER INFORMATION, Recommended Component Selections, Recommended FB Resistor Range and TAPE AND REEL INFORMATION

M BC C BC GAC	N AI EGE NC	LB B N AI	NG	N AI EC BC A GI GML	K
SCT2230MLUAR	Tape & Reel	5000	7	ECLGA2.5X1.7-7L	3

Over operating free-air temperature unless otherwise noted(1)

K M	GE	LG
V_{IN}	-0.3 to 19	V
V_{SW}	-1	



SCT2230M Top View

(2.5mm x 1.7mm)

L KC	NG	NG D LA G L
VOUT	1	Power output, please use as large an output capacitor as possible to reduce output voltage ripple
FB	2	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regu4 67 /SpaangFBe reg G[r)-3]TJETQ EMC /

V_{IN}=12V, T_J=-40℃~125℃, typical values are tested under 25℃.

K M	N KC C	C AMLBGGML	KG N K	LG
N M				
V_{IN}	Operating input voltage		4.2 17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising	4.0 350	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V	1.2	uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=12V. BST-SW=5V	220	uA
C K				
V_{EN_H}	Enable high threshold		1.215	V
V_{EN_L}	Enable low threshold		1.12	V
N KM DC				
R_{DSON_H}	High side FET on-resistance		50	mΩ
R_{DSON_L}	Low side FET on-resistance		24	mΩ
D C				
V_{FB}	Feedback Voltage	T_J=25℃, CCM	0.788 0.8 0.812	V

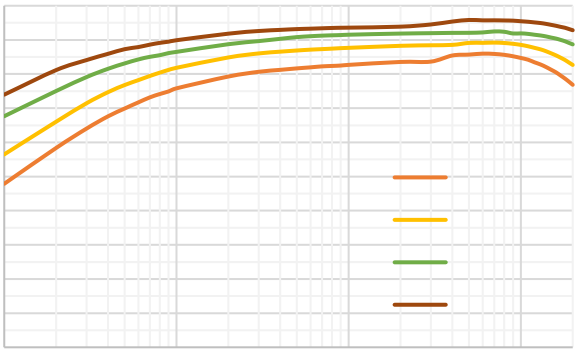


Figure 1. Efficiency vs Load Current(VIN=7.2V)

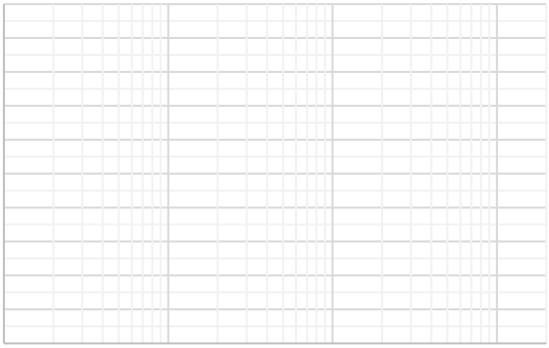


Figure 2. Efficiency vs Load Current(VIN=11.1V)

Figure 3. Load Regulation

Figure 4. FB Voltage Vs. Temperature

Figure 5. UVLO Vs. Temperature

Figure 6. Quiescent Current Vs. Temperature

M A

The SCT2230M device is 4.2-17V input, 2A output, synchronous step-down converter module with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2230M turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2230M turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} \quad \frac{V_{OUT}}{V_{IN}} \qquad (1)$$

Where:

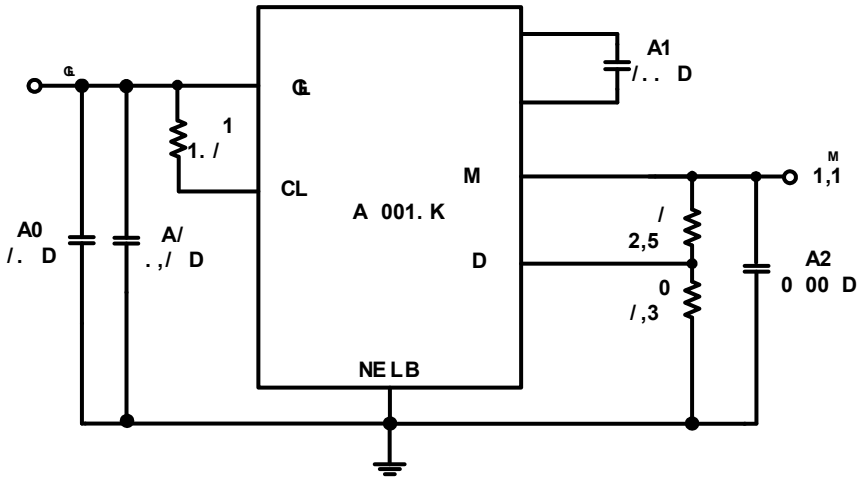
VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 220ns typical.

N K &N K

The SCT2230M is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The0ns

T97.1 0 612 792 reW* nBT/F2 9.961B<</MCID 114/Lang (en-US)>BDC q0.00000912 0 612 792 reW* nBT/F2 9.96 Tf76./L



D , / 0 G 1,1 -0 M

B N

B N	C
Input Voltage	12V
Output Voltage	3.3V
Output Current	2A
Switching Frequency	1.2MHz
Output voltage ripple (peak to peak)	25mV
Transient Response 0.5A to 1.5A load step	ΔVout = 120mV

G A

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2230M.

Use Equation (5) to calculate the input voltage ripple:

Vin=12V, Vout=3.3V, unless otherwise noted

Figure 9. Power up(Iload=2A)

Figure 10. Power down(Iload=2A)

Figure 11. EN toggle

Figure 15. Load Transient (0.2A-1.8A, 1.6A/us)

Figure 16. Load Transient (0.5A-1.5A, 1.6A/us)

Figure 17. Output Ripple (Iload=0A)

Figure 18. Output Ripple (Iload=0.1A)

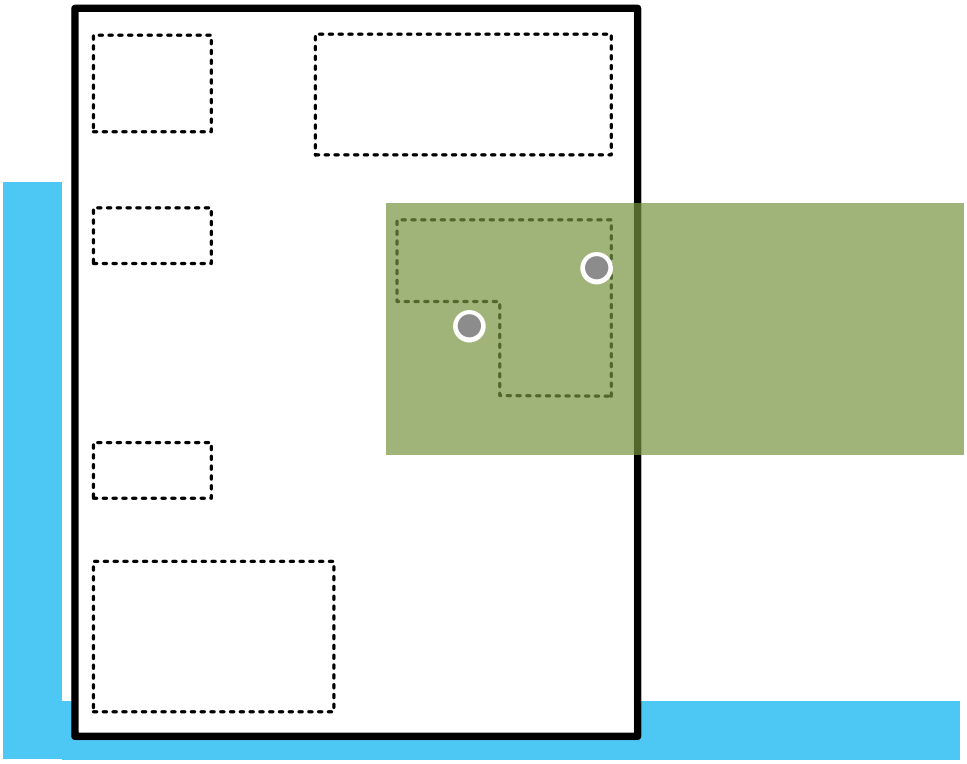
Figure 19. Output Ripple (Iload=2A)

Figure 20. Thermal, 3.3Vout/2A

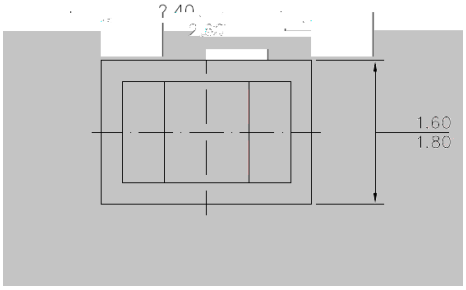
E

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21 is the recommended PCB layout of SCT2230M.

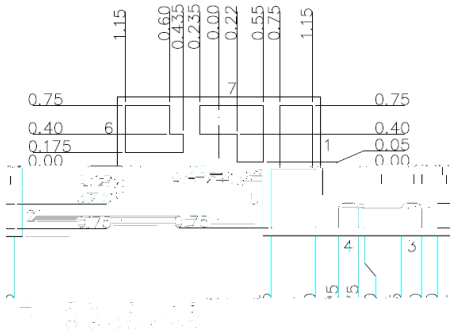
The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.



D 0/ , NA C

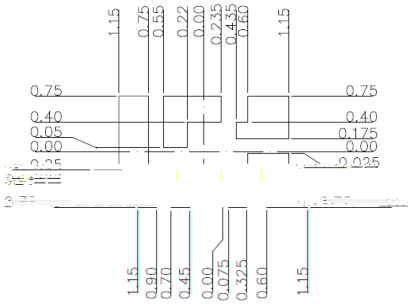


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

LM C8

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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e30 25[ )]TJETQq0.0000091495 4/GS97 63.0f7.45BT/F2 763.0.93 f7.45495 4/GS97 cs0ImageeDo Artifact /Spanhed MCID 0/Lang (e)-US